METHOD AND APPARATUS FOR CONTROLLING DATA OUTPUT FREQUENCY

ABSTRACT OF THE DISCLOSURE

Broadly speaking, a method and corresponding apparatus is provided for controlling a data output rate of an electronic device. More specifically, the method and corresponding apparatus enables an equivalent data output rate to be obtained from each of an ASIC and an FPGA prototype of the ASIC while maintaining equivalent logic between the ASIC and the FPGA prototype. A validity bit is attached to each output data signal in accordance with each cycle of a clock signal. The validity bit provides an indication as to whether the associated data signal should be processed (i.e., transmitted as output) normally. Only valid output data signals as identified by their validity bit value are transmitted. Thus, the validity bit values associated with successive data signals can be defined to generate a particular data output rate.